## REMARKS

### I. Introduction

At the time of the Office Action dated May 19, 2006, claims 1-3 were pending in this application. In this Amendment, claim 1 has been amended, and new claims 4 and 5 have been added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the written description of the specification.

### II. The Rejection of Claims 1-3

Claim 1 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Udell, Jr. in view of Chrudimsky et al. The Examiner admitted that Udell, Jr. fails to disclose a scan test method using registers, but instead, describes using flip-flops. The Examiner applied Chrudimsky et al. and asserted that the reference teaches a scan test using scan registers. Accordingly, the Examiner concluded that it would have been obvious to modify Udell, Jr. based on the teaching so Chrudimsky et al. to arrive at the claimed invention.

Applicants submit that the applied combination of Udell, Jr. and Chrudimsky et al. does not teach a technique for testability of a semiconductor integrated device including all the limitations recited in independent claim 1. Specifically, the applied combination does not teach, at a minimum, the following limitations:

> the third step of determining test signals for detecting the undetected faults;
>
> the fourth step of determining test signals most likely to meet the test signals of the third step from among the set of predetermined test signals of the fault simulation of the first step;

> the fifth step of replacing registers at the input side associated with the undetected faults of the second step with scan registers and connecting the scan registers in a scan chain thereby to construct a modified circuit; and
>
> the sixth step of conducting the fault simulation or a test by switching to the test signals determined in the fourth step at the timing corresponding to the undetected faults while using the predetermined test signals in the first step for the modified circuit.

A fault simulation is performed in a functional test. In the fourth step, a signal similar to a test signal for detecting undetected faults is determined from predetermined signals of the first step. In the fifth step, a register at an input side is changed to a scan register to provide an input value (test signal) capable of detecting faults to a test object to broaden the fault coverage. It is noted that test signals are a set of output values from a plurality of registers at an input side of a test object, as claimed.

Udell, Jr. pertains to a method for designing a scan path for a logic circuit and testing of the same. In the statement of the rejection, the Examiner asserted that Udell, Jr. discloses the third and fourth steps of the claimed invention by citing the following portion:

> The list of undetected, observable faults (block 60) is now provided to the fault simulator to identify the flip-flops where undetectable faults are observable. (bubble 66). Because some faults will be observable at more than one flip-flop and at different times depending upon the test patterns, it is preferred that a set of flip-flops be identified where all such faults are observable. This can be either all of the identified flip-flops or a subset which includes the most prominent or important of the flip-flops.

Column 4, line 63 to column 5, line 4. The above portion teaches identifying flip-flops where faults are observable. This does not teach determining test signals for detecting undetected faults in the third step, and determining test signals most likely to meet the test signals of the third step from among the set of predetermined test signals of the fault simulation of the first step, as claimed. The Examiner's comments "the test pattern is found by determining a test that will

make all faults observable" (page 3, line 3-4 of the Office Action) does not teach the above claimed steps.

The Examiner also asserted that Udell, Jr. in column 5, lines 4-8 teaches the fifth step of the claimed invention, which is reproduced below:

> The information generated during simulation (block 68) can be used to select this set of flip-flops to be connected in a scan path. (bubble 70) The designer can then design a scan path which connects the identified flip-flops.

It is apparent that this portion does not teach replacing registers at the input side associated with the undetected faults of the second step with scan registers and connecting the scan registers in a scan chain thereby to construct a modified circuit, as claimed. In other words, Udell, Jr. does not teach changing an input side, such as input testing signal or flip-flips.

Furthermore, the Examiner asserted that Udell, Jr. in column 5, lines 8-17 teaches the sixth step of the claimed invention switching to the test signals determined in the fourth step. The Examiner's cited portion is reproduced below:

> Furthermore, the simulation will determine the times during the application of the test patterns when the undetectable faults are also observable at the identified flip-flops (block 68). This information can be used to select a set of times for scanning the circuit. The set of times selected is normally a subset of the identified times, with a minimum number of scan times being chosen to permit detection of all faults. Preferably, both the number of chosen flip-flops and the number of scan times will be minimized.

The Examiner's cited portion is silent on switching testing signals between signals in the first step and signals in the fourth step, as claimed.

It is noted that the secondary reference, Chrudimsky et al., is also silent on, at a minimum, the claimed limitations discussed above.

Based on the foregoing, Udell, Jr. and Chrudimsky et al., either individually or in combination, do not teach a technique for testability of a semiconductor integrated circuit

including all the limitations recited in independent claim 1. Applicants, therefore, respectfully solicit withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) and favorable consideration thereof.

Claim 2 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Udell, Jr. and Chrudimsky et al. in further view of Maeno.

Dependent claim 2 is patentably distinguishable over Udell, Jr., Chrudimsky et al. and Maeno at least because the claim includes all the limitations recited in independent claim 1. Maeno, directed to a semiconductor integrated circuit with a scan path circuit, does not teach, among other things, the claimed third to sixth steps, and does not cure the deficiencies of the applied combination of Udell, Jr. and Chrudimsky et al. Withdrawal of the rejection of claim 2 under 35 U.S.C. §103(a) is, therefore, respectfully solicited.

Claim 3 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Udell, Jr. in view of Huang et al., Golshan and Chrudimsky et al. According to the Examiner, the applied combination of these references teaches a technique for testability of a semiconductor integrated circuit including all the limitations recited in claim 3. This rejection is respectfully traversed.

The present invention selects register groups (first or second register group) capable of observing of test data and test results by a processor or through a terminal of a semiconductor integrated circuit. Selection of register groups is important because the selection affects test quality and testing time. In response to the Examiner's rejection of claim 3, Applicants specifically submit that the applied combination of the references does not teach, at minimum, second registers that can be controlled and observed directly from a terminal of the

semiconductor integrated circuit, as recited in claim 3. It is noted that the registers are connected to a combination logic circuit.

In the statement of the rejection, the Examiner admitted that the applied combination of Udell, Jr. and Huang et al. fails to teach the claimed second registers. The Examiner, then, asserted that Golshan teaches such missing feature by citing column 1, lines 29-45, part of which is reproduced below:

> As is well known, a boundary-scan implementation allows for testing of interconnects in a board environment by loading or "scanning in" test patterns into a series of interconnected boundary-scan registers (BSRs). Each test pattern loaded in the BSRs provides a different set of control and data signals to the output drivers. The response of the output drivers to the test patterns can be captured by an adjacent circuit on the board and scanned out. To run a functional test vector, an input test pattern is scanned in through the BSRs. After one or more clock cycles, the response of the circuit can then be captured in the BSRs and either scanned out or monitored at the output pads.

Based on the disclosure of Golshan, the Examiner asserted that "the semiconductor terminal is what is scanning in the test patterns" (page 6, the third full paragraph of the Office Action).

However, Applicants stress that Golshan does not teach the claimed "second registers that can be controlled and observed directly from a terminal of the semiconductor integrated circuit." Golshan teaches that a terminal of a general boundary scan is controlled, and registers are connected in that scan chain. It is, therefore, apparent that registers in Golshan are used as a scan chain, and such registers are different from the claimed "second registers [connected to a combination logic circuit] that can be controlled and observed directly from a terminal of the semiconductor integrated circuit."

It is noted that Chrudimsky et al. does not teach, and the Examiner did not point out where in the reference teaches, the claimed second registers.

Based on the foregoing, Applicants submit that the applied combination of Udell, Jr., Huang et al., Golshan and Chrudimsky et al. does not teach a technique for testability of a semiconductor integrated circuit including all the limitations recited in claim 3. Applicants, therefore, respectfully solicit withdrawal of the rejection of claim 3 under 35 U.S.C. §103, and favorable consideration thereof.

## III. New Claims 4 and 5

Claims 4 and 5 are patentably distinguishable over the cited references at least because these claims include all the limitations recited in independent claim 1. Applicants respectfully solicit favorable consideration of claims 4 and 5.

## IV. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

for #46,692

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:TT
Facsimile: 202.756.8087
**Date: August 17, 2006**

**Please recognize our Customer No. 20277 as our correspondence address.**

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